C. U. SHAH UNIVERSITY
Wadhwan City

FACULTY OF: - Technology and Engineering
DEPARTMENT OF: - Information Technology
SEMESTER: - VIII
CODE: - **4TE08ACA1**
NAME: – **Advanced Computer Architecture**

Teaching & Evaluation Scheme: -

Subject Code	Subject Name	Teaching Scheme (Hours)				Credits	Evaluation Scheme							
							Theory				Practical (Marks)			Total
							Sessional Exam		University Exam		Internal		University	
		Th	Tu	Pr	Total		Marks	Hours	Marks	Hours	Pr/Viva	TW	Pr	
4TE08ACA1	Advanced Computer Architecture	3	0	2	5	4	30	1.5	70	3.0	-	20	30	150

Objectives:

The learning objectives of this course are to:

Describe Need of parallel and pipeline processing.
Describe Need of Advance Computer Architecture.
Describe different parallel processing architectures based on relationships between processing elements, instruction sequence, memory and interconnected network.

Prerequisites:

Basic knowledge about Computer Architecture, Operating System.

Course outline:

Sr. No.	Course Contents	Total Hrs.
1	**PROCESSOR AND MEMORY HIERARCHY:** Advance processor technology, superscalar and vector processor, Memory hierarchy technology, Virtual memory technology	08
2	**INSTRUCTION LEVEL PARALLELISM:** ILP, Concepts and challenges, Hardware and software approaches, Dynamic scheduling, Speculation - Compiler techniques for exposing ILP, Branch prediction	08

3	**PIPELINING AND SUPER SCALAR TECHNIQUES:** Liner pipeline processors, Nonlinear Pipeline processors, Instruction Pipeline design, Arithmetic pipeline design, superscalar and super-pipeline design.	**08**
4	**MULTIPROCESSORS AND THREAD LEVEL PARALLELISM:** Multiprocessors and Multicomputer, three generations of multicomputer, Symmetric and distributed shared memory architectures, Performance issues,Synchronization, Models of memory consistency, Introduction to Multithreading.	**08**
5	**MEMORY AND I/O:** Cache performance, Reducing cache miss penalty and miss rate, Reducing hit time, Main memory and performance, Memory technology. Types of storage devices, Buses, RAID, Reliability, availability and dependability, I/O performance measures, Designing an I/O system.	**08**
6	**MULTI-CORE ARCHITECTURES:** Software and hardware multithreading, SMT and CMP architectures, Design issues, Case studies, Intel Multi-core architecture, SUN CMP architecture, heterogenous multi-core processors, case study: IBM Cell Processor.	**08**
	Total	**48**

Learning Outcomes:

After completing this course, students will be able to:

Ability to describe the operation of modern and high performance computers.

Technical competence in computer architecture and high performance computing.

Ability to undertake performance comparisons of modern and high performance computers.

Ability to improve the performance of applications on modern and high performance computers.

Development of software to solve computationally intensive problems.

Books Recommended:

1. Computer architecture, A quantitative approach by **John L. Hennessey and David A. Patterson**, Morgan Kaufmann / Elsevier Publishers, 4th. edition, 2007.
2. Parallel computing architecture: Ahardware/software approach by **David E. Culler, Jaswinder Pal Singh**, Morgan Kaufmann /Elsevier Publishers, 1999.
3. Scalable Parallel Computing by **Kai Hwang and Zhi.Wei Xu,** Tata McGraw Hill, NewDelhi, 2003.
4. Advanced computer architecture by **Kai Hwang,** Tata Mcgraw Hill, 2011.